32.4 UHF RFCPUs on Flexible and Glass Substrates for Secure RFID Systems

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RFID technology is one of the key technologies of the ubiquitous computing era. However, there are still challenges left for RFIC tags, such as, realizing physical flexibility, improved security and lower cost. In response to such demands, a flexible RFCPU was recently developed using 13.56MHz RF signals (HF RFCPU) [1], which contains a flexible CPU (8b) with a wireless communication function, using flexible LSI technology [2] based on glass LSI technology [3,4] and peeling and transferring technology [2].

Since the HF RFCPU, demand continues for further sophistication of RFIC tags in order to realize a more functional RFID system, for example, in the extension of communication range, reduction in power consumption, and in the improvement of encryption (specifically, resistance to side-channel attacks). To answer these needs, a UHF RFCPU (8b) using UHF (915MHz) RF signals was designed, since long distance communication is more feasible, at least in principle, than with 13.56MHz RF signals. However, in employing UHF, there are many circuit design challenges, such as, the stable generation of clock signals. Furthermore, in order to accomodate the other requirements stated above, the overall design of the HF RFCPU itself needs to be reconsidered.

In the UHF RFCPU, the generation of clock signals with a stable frequency, unaffected by the characteristic variation of TFTs, was realized by a digital control clock generator. As well, a reduction in power consumption was achieved by improvements in the operating efficiency of the CPU and by control of the active region of the memory array. In addition, by reducing the number of transistors in the CPU and the controller, the capacity of the memory was increased at the same time as reducing chip size. By the increasing the memory capacity, the anti side-channel attack function could be realized as software to improve the encryption function.

For the UHF RFCPU, the communication specification is partially based on Auto-ID Center Class I Region 1 (North America). A design summary of the UHF RFCPU and a micrograph of the flexible UHF RFCPU is shown in Fig. 32.4.1 and Fig. 32.4.2, respectively. A block diagram of the UHF RFCPU is shown in Fig. 32.4.3. The UHF RFCPU is comprised of an RF circuits, including circuits such as a power supply, a demodulator and modulator, a clock generator, as well as logic circuits including a CPU, a controller, a ROM, and RAM. The power supply consists of a rectifier and a capacitor. The demodulator is comprised of a rectifier and a LPF, and extracts data from the RF signals. Finally, the modulator superimposes sending data over RF signals using Manchester coding.

A block diagram of the digital control clock generator and its main signal waveforms are shown in Fig. 32.4.4 and Fig. 32.4.5, respectively. The digital control clock generator consists of a regulator, a ring oscillator (RO) and counters (a master counter, a slave counter, a divide counter and a PH counter). The regulator generates a constant voltage from the power supply voltage, and supplies it to the RO. Then, the RO generates a ring oscillator clock CLK_{RO} whose frequency is to be f_{ROS} (f_{RONS}) during a SYNC (non-SYNC) term. The master counter generates master reset signals RST_{MASTER} in the SYNC term, from SYNC signals that are asserted from the demodulator with a cycle T_0, as well as counts the rising edge number n_{T0} of CLK_{RO} with RST_{MASTER} as the reset signals. Note that the following is satisfied: $(n_{T0}-1)/f_{ROS} < T_0 < (n_{T0}+1)/f_{ROS}$. The slave counter generates slave reset signals RST_{SLAVE} every time n_{T0} rising edge numbers of CLK_{RO} are counted in the non-SYNC term. In other words, RST_{SLAVE} consists of pulse signals with a cycle $T_{0NS}=n_{T0}/f_{RONS}$. In the divide counter, CLK_{RO} is frequency divided by a division ratio $m=INT(n_{T0}/n_{SYS})$, and this becomes the system clock CLK_{SYS}. The PH counter is driven by CLK_{SYS} with PH reset signals $RST_{PH}=(RST_{MASTER}|RST_{SLAVE})$ as the reset signals and generates clock signals PH1/PH2 of the logic circuit. Note that after asserting RST_{PH}, each of the clock signals PH1/PH2 toggles $2n_{PH}$ times. In other words, in the SYNC (non-SYNC) term, clock signals PH1/PH2 with an average frequency of $<f_{PHS}>=n_{PH}/T_0$ ($<f_{PHNS}>=n_{PH}/T_{0NS}$) is obtained. Note that in the UHF RFCPU, T_0=14.25ms, n_{T0}~256, n_{SYS}=64, f_{PH}=1.12MHz, n_{PH}=16, and $f_{ROS,\ RONS}$~18MHz are employed.

By the relationship between T_0 and T_{0NS}, a relationship where $(1-1/n_{T0})\cdot(f_{ROS}/f_{RONS}) < (<f_{PHNS}>/<f_{PHS}>) < (1+1/n_{T0})\cdot(f_{ROS}/f_{RONS})$ is obtained. In other words, by making the frequency change of CLK_{RO} in the SYNC term and the non-SYNC term small as well as by increasing n_{T0} (that is, increase the frequency of CLK_{RO}), the frequency precision of PH1/PH2 can be improved regardless of the characteristic variations found in TFTs. In the UHF RFCPU, by supplying the power supply voltage of the RO from the regulator, the frequency change of CLK_{RO} is reduced.

The 8b CISC CPU was changed (relative to HF RFCPU) to improve the operation efficiency by about 4×, and the implementation area was reduced by about 25%. Note that performance was improved by about 1.5× at the same time as both reducing the clock frequency by 1/3 (1.12MHz) and reducing the power consumption. Furthermore, the number of transistors in the controller was reduced by about 30% compared to the HF RFCPU.

A 4KB mask ROM stores programs, ID numbers, etc. In the ROM, a reduction in power consumption is achieved by segmentation of the bit line that is precharged during reading. A 512B SRAM is used as the work area of the CPU in addition to being used as a memory-mapped register. The SRAM is divided into 16 sub-blocks, and by having a structure in which only one sub-block is active during reading/writing, power consumption is reduced. Power consumption of the memory as a result is about 1/4 of the HF RFCPU, even though the capacity of the ROM and SRAM were increased by 2× and 8×, respectively, relative to the HF RFCPU. By increasing the memory capacity, the anti side-channel attack function was able to be realized in software to improve the encryption function. Note that the encryption routine employs DES and the Transformed Masking Method [5] is employed as the anti side-channel attack routine.

Measurement results for the UHF RFCPU are shown in Fig. 32.4.6. In the measurement, the RF communication signals (915MHz) are output from the antenna, and then the response signals from the UHF RFCPU are captured by a spectrum analyzer. The measurement result in Fig. 32.4.6 is a result of measuring the response signal waveform of the glass UHF RFCPU by the spectrum analyzer. The maximum communication range is 43cm when the antenna output is 9dBm. The power consumption within the chip is 0.54mW when the power supply voltage is 1.5V. This is about 1/7 of the power required by the HF RFCPU.

References:

[1] H. Dembo, et al., "RFCPUs on Glass and Plastic Substrates Fabricated by TFT Transfer Technology," *IEDM Tech. Dig.*, pp. 1067-1069, Dec., 2005.
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[3] B. Lee, et al., "A CPU on a Glass Substrate Using CG-Silicon TFTs," *ISSCC Dig. Tech. Papers*, pp. 164-165, Feb., 2003.
[4] T. Ikeda, et al., "Full-Functional System Liquid Crystal Display Using CG-Silicon Technology," *SID Dig. Tech. Papers*, pp. 860-863, May, 2004.
[5] M. Akkar, and C. Giraud, "An Implementation of DES and AES, Secure Against Some Attacks," *Proc. CHES, Springer LNCS 2162,* pp. 309-318, May, 2001.

UHF RFCPU	Technology			LTPS TFT 0.8μm Peeling and Transferring Gate + 1 Metal Layer
	Transistor count			133k
	Core size (W X H X T)			10.5mm x 8.9mm x 145μm
	Weight *			262mg
	RF circuit		Components	Power supply Demodulator Modulator
	Clock generator		Components	Regulator Ring oscillator Counters
	Logic circuit	CPU	Tr count	20k
			Clock freq.	1.12MHz
			Architecture	8b CISC
		ROM	Size	4KB
		RAM	Size	512B
		Controller	Tr count	10k
			Components	CPU interface RF interface Memory controller

* Antenna is not included

Figure 32.4.1: Design summary.

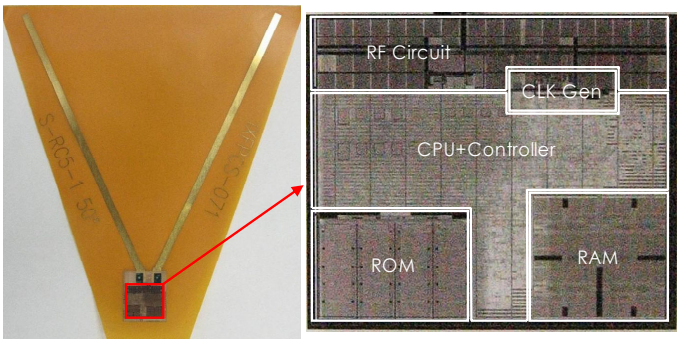

Figure 32.4.2: Micrograph of the flexible UHF RFCPU.

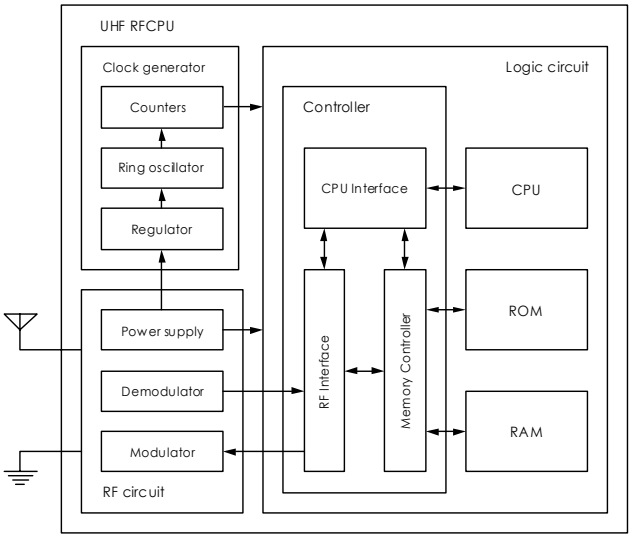

Figure 32.4.3: Block diagram.

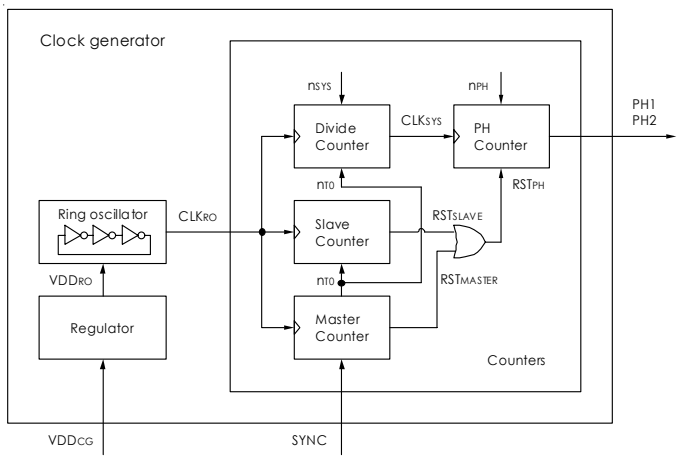

Figure 32.4.4: Block diagram of the digital control clock generator.

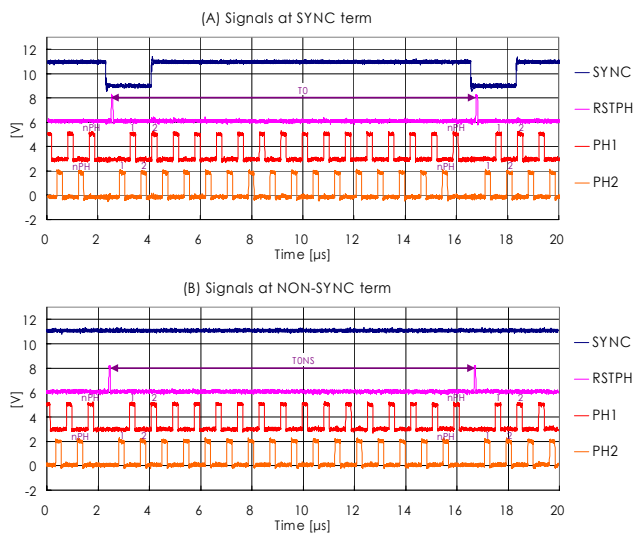

Figure 32.4.5: Signal waveforms of the digital control clock generator.

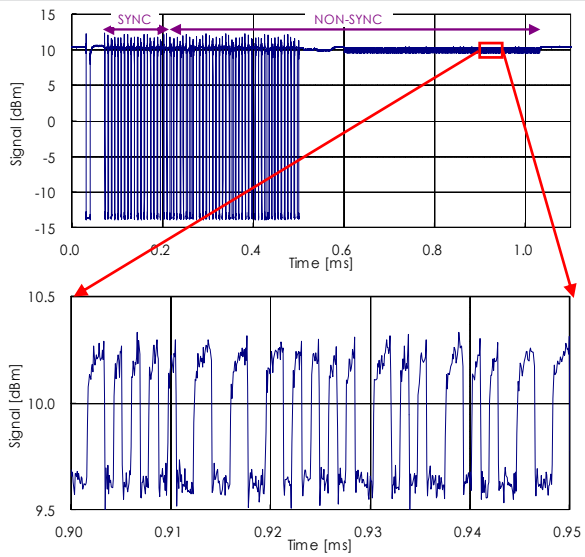

Figure 32.4.6: Measurement results.